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# ABSTRACT OF THE DISCLOSURE

There is described an improved semiconductor device of  
5 chip-scale package (CSP) comprising posts provided on respective  
electrode pads of a semiconductor chip, and solder balls which  
are provided on the respective posts as external terminals after  
the semiconductor chip has been encapsulated with resin while  
the posts are held in a projecting manner. The semiconductor  
10 device prevents occurrence of cracks, which would otherwise  
be caused by stress which is induced by a difference in coefficient  
of linear expansion between the semiconductor chip and the  
sealing resin and is imposed on the posts. In order to alleviate  
the stress imposed on the posts, a stress-absorbing layer formed  
15 from a metal layer having a low Young's modulus, such as gold  
(Au) or palladium (Pd), is interposed in the middle of each  
of the posts.